REMARKS

The Abstract and Specification have been amended to correct informalities. No new matter has been added.

Claims 10, 15 and 19 have been amended to correct informalities. No new matter has been added.

Attached hereto is a marked-up version of the changes made to the Abstract, Specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

Respectfully submitted,

James J. Maune
PTO Reg. No. 26,946
Attorney for Applicant
(212) 408-2566

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

The abstract has been amended as follows:

The invention relates to a method and an arrangement for instruction word generation in the [driving] controlling of functional units in a processor, the instruction words comprising a plurality of instruction word parts. In this case, in a program sequence, under the control of a program word, an instruction word is taken from a row – determined by a reading row number – of an instruction word memory that can be written to row by row, the said instruction word is altered by means of substitution of an instruction word part by the information part of the respective program word and is written back to a row of the instruction word memory, the said row being determined by a writing row number. Afterwards, an instruction word – which is generated in this way and is to be executed in accordance with the program – for controlling the functional units is output to the processor.

The title has been amended as follows:

METHOD AND ARRANGEMENT FOR INSTRUCTION WORD GENERATION IN THE [DRIVING] CONTROLLING OF FUNCTIONAL UNITS IN A PROCESSOR

Paragraph 1 has been amended as follows:

The invention relates to a method for the generation of instruction words for driving functional units in a processor, the instruction words comprising a plurality of instruction word parts. Each instruction word part respectively [drives] controls a functional unit. A sequence of primary instruction words, which originate from a translation of a program code, undergoes

fractionation into program words [before] of a program sequence. During the program sequence, under the control of a program word which has an information part at least of the width of an instruction word part, an instruction word is taken from a row – determined by a reading row number – of an instruction word memory that can be written to row by row and is altered by means of substitution of an instruction word part with the information part of the respective program word. It is then written back to a row of the instruction word memory, the said row being determined by a writing row number. After generation – effected in this way – of an instruction word corresponding to the primary instruction word to be executed, the instruction word is provided to an output for driving the functional units.

Paragraph 3 has been amended as follows:

The German Patent Specification DE 198 59 389 C1 describes an arrangement for [driving] controlling functional units in a processor. As discussed therein, the program word contains, in addition to an information part, at least also the information about the writing and reading row numbers for the instruction [work] word memory. This necessitates a large width of the program words which, on the one hand, with the requisite processing and decoding of the control information, produce limitations in the processing speed of the task-related data. On the other hand, the high data width of the program word processing necessitates high outlay on hardware in the realization of the processor.

Paragraph 16 has been amended as follows:

In a further advantageous embodiment of the methods according to the invention, it is provided that an interrupt signal immediately triggers, at the processor, while processing a first

task using one instruction word page, the execution of the interrupt second task on the other instruction word [memory] memory page whereby after the completion of the interrupted second task, processing of the first task can be resumed using the processing state of the said first task in the one instruction word memory page.

In the Claims:

10. (Once Amended) A method for generation of instruction words in a digital processor having an instruction word memory wherein instruction words are arranged in rows, each instruction [would] word having a plurality of instruction word parts, each driving a functional unit of said processor, comprising:

deriving primary instruction words from a program code;

[assembling] combining said primary instruction words into a sequence of associated program words;

reading an instruction word from a row of said instruction word memory determined by a reading row number;

modifying said read instruction word by substituting an [instructin] instruction word part with an information part of an associated program word;

writing said modified instruction word part to a row of said instruction word memory determined by a writing row number; and

outputting a completed [nstruction] instruction word to drive said functional units of said processor;

wherein said reading row number and said writing row number are provided by respective reading row and writing row registers, and wherein a number of sequential reading row and writing row numbers are determined by contents of a block length register.

15. (Once Amended) A method for the generation of instruction words in a digital processor having an instruction word memory wherein instruction words are arranged in rows, each instruction word having a plurality of instruction word parts, each driving a functional unit of said processor, comprising:

deriving primary instruction words from a program code;

assembling said primary instruction words into a sequence of associated program words;

reading an instruction word from a row and page of said instruction word memory determined by a reading row number and a page number stored in a page register;

modifying said instruction word by substituting an instruction word part with an information part of an associated program word;

writing said modified instruction word to a row and page of said instruction word memory determined by a writing row number and a page number stored in said page register; and

outputting a completed instruction word to [drive] control said functional units of said processor.

19. (Once Amended) The improvement specified in claim 18 wherein said address generation unit includes a read pointer register, an associated read pointer up/down counter, a write pointer register and an associated write pointer up/down counter, wherein said counters provide ring counting in accordance [wit] with the contents of a block length register.